OLLSCOIL NÁISIÚNTA NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

Summer Examinations 2014

CS4403 Introduction to Embedded Systems

Professor I. Gent
Professor B. O'Sullivan
Dr J. G. Vaughan

Answer QUESTION 1 and ONE other QUESTION

Total Marks: 80

1.5 Hours

The use of electronic calculators is permitted

PLEASE DO NOT TURN THIS PAGE UNTIL INSTRUCTED TO DO SO

ENSURE THAT YOU HAVE THE CORRECT EXAM PAPER

QUESTION 1 (48 Marks)

(a) A, B and C are memory variables. R2, R3 and R4 are registers in the register file. Load, Add and Store are ISA commands in a RISC architecture. Write down the sequence of ISA-level instructions that implements the high-level language statement C = A + B

4 Marks

(b) Describe briefly how a memory operand can be addressed in a generic RISC computer Load instruction. Give one example. **4 Marks**

(c) Describe briefly what is being done by the following RISC code sequence

```
        Load            R2, N
        Clear           R3
        Move            R4,#NUM1
LOOP:   Load            R5,(R4)
        Add             R3,R3,R5
        Add             R4,R4,#4
        Subtract        R2,R2,#1
        Branch_if_[R2]>0  LOOP
        Store           R3,SUM
```

4 Marks

(d) Write down the sequence of instructions that will put the 32-bit value 0x20004FF0 in register R2. Why is more than one instruction needed to do this? **4 Marks**

(e) A keyboard input interface has a status register KBD_STATUS in which bit 1 is set when a character is received from the keyboard and cleared when KBD_STATUS is read by a program. Write an instruction loop, READWAIT, to wait for an appropriate keyboard status before reading a character from KBD_DATA. **4 Marks**

(f) A keyboard input routine, READCHAR, is executed when an interrupt is received from the keyboard. Briefly outline the structure of the routine and the difference between it and the approach in part (e) above. **4 Marks**

(g) Interrupt routine READCHAR needs to use registers R2 and R3 to contain a buffer address PNTR and the contents of KBD_DATA respectively. Write the instruction sequence to save these registers on the stack, put the PNTR and KBD_DATA values in the registers and save the character in the buffer addressed by PNTR. You may assume that the stack pointer, SP, has already been initialised.

4 Marks

(h) Describe, in words, the five steps into which execution of the instruction

Load R5, X(R7)

can be subdivided **4 Marks**

(i) List the 5 actions into which execution of a general instruction can be divided. List the five corresponding hardware stages. **4 Marks**

(j) Show in one diagram a conceptual view of the data path (ALU, register file) for computational and immediate instructions. **4 Marks**

(k) Write a short paragraph on oscilloscope probe compensation as practised in your laboratory sessions. Sketch overcompensated, undercompensated and correctly compensated waveforms. **4 Marks**

(l) List the actions necessary in order to start up and run the Arduino Due "Blink' example. **4 Marks**

QUESTION 2 (32 Marks)

Use the following code sequence in part (a) of this question:

```
1. int sensorPin = A0;
2. int ledPin = 13;
3. int sensorValue = 0;
4. void setup() {
5.      pinMode(ledPin, OUTPUT);
6.      }
7. void loop() {
8.      sensorValue = analogRead(sensorPin);
9.      digitalWrite(ledPin, HIGH);
10.     delay(sensorValue);
11.     digitalWrite(ledPin, LOW);
12.     delay(sensorValue);
13.     }
```

(a) Explain what this program does when it is uploaded to an Arduino card. Explain the purposes of lines 4, 9 and 5. What external circuitry would you use in connection with this sketch and how would you connect it? **9 Marks**

(b) The Arduino Due is based on an Atmel AT-SAM3X8E processor which itself contains an ARM Cortex M3 core. What is the maximum clock rate of the SAM3X? Describe the physical memory available on the Arduino AT-SAM3X. What is bit banding, as supported by the Cortex M3? What advantages does it provide for the real-time programmer? **9 Marks**

(c) Describe the register architecture of the ARM Cortex-M3 **7 Marks**

(d) Describe the ARM Cortex-M3 Memory Map **7 Marks**

QUESTION 3 (32 Marks)

(a) The Intel Galileo board is an Arduino-compatible system based on the Intel Quark SoC X1000 Core. What is the maximum clock frequency of the Quark? On what architectural philosophy is it based? Give an overview of the memory layout. Draw a block diagram of the address translation mechanism.

10 Marks

(b) Give an account of the memory organization of the Quark processor. **10 Marks**

(c) Based on your experience and knowledge of RISC and CISC processor design, write a short technical essay comparing the Intel Quark with the ARM M3 from the point of view of suitability for use in embedded systems. You may construct your arguments as a series of bullet points. You are allowed to favour either processor or neither, so long as you provide good reasons for your opinions.

12 Marks

PLEASE DO NOT TURN THIS PAGE UNTIL INSTRUCTED TO DO SO.

THEN ENSURE THAT YOU HAVE THE CORRECT PAPER.